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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,872	06/28/2001	Tatsuya Shimoda	109975	3054

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EXAMINER
BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/892,872	Applicant(s) Shimoda et al.
	Examiner B. William Baumeister	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 31, 2003*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above, claim(s) *7, 11, and 17* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-6, 8-10, 12-16, and 18-25* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Dec 19, 2002* is: a) ☒ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-6, 8-10, 12-16 and 18-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith et al. '186 (supplied in IDS, paper #3) in view of Applicant's Prior Art Admissions.

a. Smith discloses shaped microstructures that are assembled into appropriately-shaped binding-site receptor recesses formed in a substrate through fluid transport (e.g., ABSTRACT). Smith teaches that the microstructures may support a wide range of devices such as diodes, transistors, integrated circuits, display devices, etc. (e.g., col. 1, lines 30-34). Smith further teaches that the microstructures are not limited to GaAs, but may also comprise, *inter alia*, other material systems such as Si, other group-IV, III-V or II-VI material systems (col. 4, lines 55). Also, the substrate on which the microstructures are assembled may be composed of Si or GaAs wafers, plastic sheets (e.g., a photocurable resin), glass or ceramic substrates, or "almost any type of material capable of forming recessed regions or generally binding sites or receptors thereon which complement the shaped blocks." (Col. 14, lines 18-24 and col. 13, lines 60-62 which specifically recites molded plastic sheets). Smith teaches that applications which require a number of different larger circuits could be realized by etching the microstructures into specific

shapes and assembling them into matching recessed regions (col. 11, lines 38-44). **Further, Smith also teaches that the microstructure may be electrically connected to the host substrate.** See e.g., FIG 11 wherein the microstructure is electrically connected to the substrate 125 by means of ring-electrode 135, and wherein electrode 131 extends across the surface of the substrate 125, isolated therefrom by insulating layer 133. Smith does not teach that ferroelectric-capacitor passive matrix arrays and/or associated peripheral circuits, specifically, may be employed within the Smith microstructure-on-substrate invention.

b. Applicant admits that ferroelectric capacitor passive matrix arrays (ferroelectric PMAs) operated by peripheral circuits are known, and that both can be grown on Si substrates. (See the BACKGROUND OF THE INVENTION section of the specification.) Applicant also acknowledges that the manufacture of integrated FEPMAs with peripheral-circuit MOS transistors was known and that it was known that this integration poses the drawback of less than optimal device performance (paragraphs [0009]-[0011]). Note particularly prior-art Figs 26A-C and the associated discussion of the prior-art FIGs in paragraphs [0003]-[0008] wherein Applicant acknowledges that it was known to electrically interconnect the drain 13 of the peripheral transistor (line driver circuit) and the PMA.

c. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have grown the conventional FEPMAs and peripheral circuits separately and integrate them onto a common substrate through the microstructure techniques taught by Smith for the purpose of obviating the device performance drawbacks which applicant acknowledges

were known. Further, it would have been obvious to one of ordinary skill in the art at the time of the invention that either specific one of the FEPMA or the peripheral circuit could be formed on a microstructure or substrate, respectively, or that both could be formed on separate microstructures and respectively assembled to a substrate, and that undertaking any particular one of these options would not produce any unexpected results; but rather, the specific option chosen would merely be determined by conventional manufacturing considerations such as (1) the space and layout requirements for the respective options; (2) the amount of wirebonding respectively required; (3) the application for which the memory device is ultimately to be employed, which in turn, would dictate such considerations as what other devices/circuits are to be integrated on or connected to the substrate and/or microstructure(s), the amount of memory required (dictating how many FEPMAs are required) and whether an inexpensive or flexible plastic would be useful as a substrate. It would have further been obvious to have electrically interconnected the peripheral circuit to the FEPMA as taught by Applicant's prior art admissions so that the device would operate as intended.

d. Regarding the newly added limitations that the microstructure is centrally located and that the peripheral circuit is peripherally positioned, the fact that the prior-art drive/control circuit is called a "*peripheral* circuit" indicates that it is positioned peripherally to the centrally located PMA. Alternatively, even assuming *arguendo* that the prior-art admission must be read so narrowly as not sufficiently disclosing that the PMA is positioned centrally and that the peripheral circuit is located peripherally, the specific positioning of the components does not

produce any unexpected results. Rather, the specific position of the respective components ultimately chosen is merely dictated by conventional considerations such as the column-row grid layout of prior-art PMA structure and the conventional means of minimizing the space required to route interconnects from the peripheral/drive circuits to the PMA. *See e.g., Lemelson v. Synergistics Research Corp.*, (DC SNY) 4 USPQ2d 1927, 1934 for the proposition, "[i]t is well settled that more than mere change of form or rearrangement of parts is necessary for patentability. *Span-Deck, Inc. v. FabCon, Inc.*, 677 F.2d 1237, 1244 [215 USPQ 835, 840-841] (8th Cir.) (citing cases), cert. denied, 459 U.S. 981, 103 S.Ct. 318 (1982); *Sheldon Friedlich Marketing v. Carol Wright Sales*, 219 U.S.P.Q. 883, 888 (S.D.N.Y. 1983)."

e. With respect to claim 9, the Examiner notes that "a microstructure" reads on a Si chip. As such, the claim recitation--that the FEPMA and the peripheral circuit are integrated on a single microstructure--reads on Applicant's prior art FIGs 24-26A/C. Similarly, claims 10 and 18 read on a microstructure that is assembled on a Si substrate; and the language "a part of the second microstructure to be integrated" (e.g., claim 10, line 6) merely sets forth the intended use of a Si chip. As such, the claim is rendered obvious by a microstructure on a Si chip so long as the chip is *capable* of, in turn, being integrated onto some other substrate (e.g., a piece of plastic or a PCB).

3. Claim 1-6, 8-10, 12-16 and 18-25 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Smith/Applicant's prior-art-admissions as applied to the claims above, and further in view of WO '170 (previously made of record in IDS #3).

a. Assuming arguendo that Applicant's above-noted prior art admissions must be read so narrowly as not sufficiently disclosing that the peripheral transistor to which the PMA is interconnected is specifically a part of a line driver circuit, WO '170 (which Applicant acknowledges is conventional or prior art in paragraph [0003] of the specification) teaches PMAs electrically interconnected to peripheral circuits that are driver circuits (e.g., page 7, lines 11-18). It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed a driver circuit for the peripheral circuit for the purpose of driving the PMA as taught by WO '170.

Response to Arguments

4. Applicant's arguments filed 7/31/03 have been fully considered but they are either moot in light of the new grounds of rejection or alternatively are not persuasive for the reasons set forth hereinabove and as follows.

a. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the

time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

INFORMATION ON HOW TO CONTACT THE USPTO

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. WILLIAM BAUMEISTER
PRIMARY EXAMINER

B. William Baumeister

Primary Patent Examiner, Art Unit 2815

August 15, 2003